PRELIMINARY REMARK

The Applicants note that page 5 of the action recites that the Action is made final. The Applicants believe that this is a typographical error, because the present action develops a new rejection of claim 6 whereas claim 6 was not amended in response to the previous action. If the Examiner really made the present action final, the Applicants respectfully request the Examiner to withdraw the finality of the action in view of the present remark.

REMARKS

Rejections under 35 U.S.C. 102

Claims 1 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,210,437 to Sawada. Applicants respectfully disagree.

Claim 1

The Examiner opines that "Sawada clearly discloses (see, for example, FIG. 2E) a well 25 that is formed by the doping of phosphorous that is material and tangible in the structure. Nowhere in the disclosure does Sawada state that this well would 'not be there' when any reasonable voltage is applied to circuit. In fact, it would be expected that such a structure would remain permanently in the structure and there is no reason suggested by Sawada to expect otherwise". The Examiner further opines that "Sawada clearly shows a distinct well structure that is in the final device embodiment of FIG. 2E. Since the entire structure (i.e. gate, source, drain, well) of Sawada is essentially identical

to the structure (also containing a gate, source, drain, well) shown in Figure 2 of the Applicant's figure with the same positioning, it would be concluded that both structures would have the same electrical functions/effects". The Examiner concludes by opining that "whether the transistor operates differently as argued by the applicant, this does not structurally differentiate the applicant's claims from what is disclosed in Sawada".

The Applicants respectfully disagree with the Examiner.

Fig 2E of Sawada shows a structure having a well 25, wherein "the well 25 has a substantially semi-circular section and is appropriate for threshold voltage control" (col. 3, lines 37-39). This relates to claim 1 of Sawada, which recites "a well layer formed in and extending below said channel region to control a threshold voltage of said MOS transistor, said well layer having a substantially semi-circular section with a non-flat lower surface and non-flat sides".

As detailed in the response filed on September 13, 2006 in reply to the action issued on June 15, 2006, Sawada teaches selecting the impurity concentration of the well 25 to provide an electrical path between the source and drain until a threshold voltage (smaller than, or equal to, a regular threshold voltage) is applied to the circuit. This teaches against a circuit as recited in claim 1, and in particular "*wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*".

Further, as detailed in the response filed on February 19, 2007 in response to the action issued on November 27, 2006, Sawada claims that well 25 allows controlling the operation of a transistor. If well 25 were somehow reading on a well as recited in claim 1, and in particular "*wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*", then the

structure of Sawada would not operate as a transistor. Thus, the language of the claims of Sawada also evidences that the well 25 does not anticipate the well of claim 1, contrary to the assertion of claim 1.

The Applicants note that by refraining from providing, as requested in the response to the previous action, an affidavit or declaration setting forth specific factual statements and explanation to support that a "transistor" reads on a structure that provides an electrical path regardless of any reasonable voltage applied to it, the Examiner has acknowledged that a "transistor" does not read on a structure that provides an electrical path regardless of any reasonable voltage applied to it.

The Examiner opines that "Sawada clearly discloses (see, for example, FIG. 2E) a well 25 that is formed by the doping of phosphorous that is material and tangible in the structure. Nowhere in the disclosure does Sawada state that this well would 'not be there' when any reasonable voltage is applied to circuit".

The Applicants have never argued that the well 25 would "not be there" when any reasonable voltage is applied to circuit. Claim 1 recites "*wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*". The skilled reader readily understands that a well can be implanted below a gate of a circuit between a drain and a source (i.e. 'be there') and still not provide an electrical path between the drain and source regardless of any reasonable voltage applied to the circuit. This is actually how depletion MOS transistors operate daily. Further, as detailed above, Sawada teaches against the well 25 providing "*an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*".

As to the Examiner opining that "since the entire structure (i.e. gate, source,

drain, well) of Sawada is essentially identical to the structure (also containing a gate, source, drain, well) shown in Figure 2 of the Applicant's figure with the same positioning, it would be concluded that both structures would have the same electrical functions/effects": the Applicants note that such assertion is not consistent with the teachings of Sawada.

Indeed, as detailed above the structure of Sawada does not operate as the claimed structure. This is evidenced both by the specification of Sawada, which describes precisely the function of well 25, and by the claims of Sawada, which recite that the well belongs to a transistor.

As to the Examiner opining that "whether the transistor operates differently as argued by the applicant, this does not structurally differentiate the applicant's claims from what is disclosed in Sawada": the Applicants respectfully note that the above assertion is nonsensical.

How could the transistor of Sawada operate differently from the claimed structure if the transistor of Sawada and the claimed structure were not structurally different? As evidenced above, the structure of Sawada does not operate as the claimed structure. Since the structures operate differently, they have necessarily a different structure.

At least in view of the above, the Applicants respectfully submit that claim 1 is novel over Sawada.

The Applicants also respectfully submit that the Examiner has failed to show that Sawada would suggest in any manner a first well that provides "*an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit*" as recited in claim 1, whereby claim 1 is also non obvious over Sawada.

Claim 5

Claim 5 depends on claim 1. Applicants respectfully submit that at least in view of its dependency on claim 1, claim 5 is patentable over Sawada.

Rejections under 35 U.S.C. 103

Claims 2, 3 and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada in view of U.S. Pat. No. 3,938,620 to Spadea, and claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,811,340 to Park in view of U.S. Pat. No. 4,145,701 to Kawagoe. Applicants respectfully disagree.

Claims 2, 3 and 4

Claims 2, 3 and 4 depend directly or indirectly on claim 1. Applicants note that the Examiner has failed to show that Spadea shows a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. In view of the above, Applicants submit that the Examiner has failed to show that Sawada or Spadea, alone or in combination, would have led one of ordinary skill to a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of any reasonable voltage applied to said circuit"*. Accordingly, Applicants respectfully submit that claim 1 is patentable over Sawada in view of Spadea, and respectfully submit that at least in view of their dependency on claim 1, claims 2, 3 and 4 are patentable over Sawada in view of Spadea.

Claim 6

The Examiner opines that Park shows the features recited in claim 6, except for the first well of the first conductivity type recited in claim 1, and opines that "it would have been obvious for one of ordinary skill in the art at the time of invention to have a first well of a first conductivity type in order to have a high density of integration".

The Applicants respectfully disagree with the Examiner.

Kawagoe teaches, in a large scale integrated circuit wherein insulated gate field-effect transistors are arrayed in the shape of a matrix, using some depletion type transistors in combination with some enhancement type transistors, so that a very large number of contact holes which are otherwise required for electrical connection between aluminum wiring and the drain regions become unnecessary. It is the reduction of the number of contact holes that permits the density of integration of the integrated circuit to be raised.

Park discloses single enhancement transistors.

The Applicants note that the Examiner has failed to show how or why introducing a first well of a first conductivity type in a single transistor of Park would in any manner allow having "a high density of integration" as asserted by the Examiner. Accordingly, the Examiner has failed to show that the skilled person would have had any motivation to amend the transistor of Park in view of the matrix of Kawagoe.

For completeness of analysis, the Applicants note that the Examiner has also failed to show that one skilled in the art would have had any motivation to amend the matrix of Kawagoe in view of the transistor of Park.

Park discloses an enhancement transistor wherein the regions 21, deemed by the Examiner to read on the plurality of wells of claim 6, are "effectively preventing punchthrough" (column 7, lines 59-62).

Park teaches (column 1, lines 39-47) that in MOS devices having a reduced channel length for high integration and high speed: "*due to the short channel length, a drain depletion region increases and interacts with a channel junction, thereby causing drain induced barrier lowering (DIBL). Further, a leakage current increases because of the punchthrough between the two depletion regions caused by the severe encroachment of the source and drain depletion regions*".

The Examiner has failed to show that in a depletion transistor, such as in Kawagoe, there would be a similar encroachment of the source and drain depletion regions that would create a similar punchtrough problem. The Examiner has also failed to show that if such similar punchtrough problem existed in the depletion transistors of Kawagoe, it would also be solved by regions such as the regions 21 of the enhancement transistor of Park.

Should the Examiner opine that there could exist a motivation to introduce such regions in the depletion transistors of the matrix of Kawagoe by relying on knowledge on his own to assert that regions such as the regions 21 of the enhancement transistor of Park would be of any use in the depletion transistors of Kawagoe, the Applicants respectfully request the Examiner to provide an affidavit or declaration setting forth the specific factual statements and explanation to support the assertion, in compliance with 37 CFR 1.104(d)(2).

It follows from the above that, even considering *arguendo* that one skilled in the art had, for an undisclosed reason, decided to modify the matrix of Kawagoe in view of Park, one would have obtained the matrix of Kawagoe wherein the enhancement

transistors would be as the enhancement transistor of Park. There is however no suggestion as to why the depletion transistors of such hypothetical matrix would differ from the transistors of Kawagoe, and in particular as to why the depletion transistors of such matrix would comprise regions such as the regions 21 of the enhancement transistor of Park.

Accordingly, even the hypothetical matrix obtained by a combination of the teachings of Park and Kawagoe would not have read on a circuit as claimed in claim 6, and in particular comprising "*a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second conductivity type are separated from said first well*".

At least in view of the above, the Applicants respectfully submit that claim 6 is non obvious in view of Park and Kawagoe.

* * *

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being electronically filed by E-Web in the United States Patent and Trademark Office on

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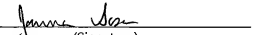
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